

CLAIMS

What is claimed is:

- 1 1. A method in a memory having a bad memory cell, the
2 method comprising:
3 testing the memory to determine the location of
4 the bad memory cell;
5 mapping out an address location associated with
6 the bad memory cell; and
7 offsetting the physical address locations
8 associated with good memory cells so that logical
9 addressing is linear and the memory appears contiguous.
- 1 2. The method of claim 1, wherein
2 the memory is within an integrated circuit and the
3 testing is self-testing performed on chip by a built in self
4 tester.
- 1 3. The method of claim 1, wherein
2 the memory is organized into one or more clusters, each
3 of the one or more clusters having one or more memory
4 blocks, and
5 the mapping out of the address location maps out a
6 memory block having the bad memory cell.
- 1 4. The method of claim 3, wherein
2 the offsetting of the physical address locations of
3 good memory cells is by one memory block corresponding to
4 the size of addressable space of the memory block having the
5 bad memory cell.
- 1 5. The method of claim 4, wherein

2 each good memory block, addressable in ascending order
3 after the memory block having the bad memory cell, has its
4 physical address locations offset by the size of addressable
5 space in a memory block to linearize the logical addressing.

1 6. The method of claim 3, wherein
2 there are four clusters having each having four memory
3 blocks and each memory block contains 512 kilobits of memory
4 cells.

1 7. The method of claim 1, wherein
2 the testing writes one or more test patterns into
3 memory cells in the memory, reads out data from the memory
4 cells, and compares read out data with the expected pattern
5 of the one or more test patterns to determine the location
6 of the bad memory cell.

1 8. The method of claim 7, wherein
2 the location of the bad memory cell is associated with
3 an address.

1 9. The method of claim 1, wherein
2 the memory is organized into one or more clusters, each
3 of the one or more clusters having one or more memory
4 blocks,
5 one or more bad memory cells are located within one or
6 more respective memory blocks, and
7 the mapping out of the address location maps out the
8 one or more respective memory blocks having the one or more
9 bad memory cells.

1 10. The method of claim 9, wherein
2 the offsetting of the physical address locations of
3 good memory cells is by one or more memory blocks associated

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- 4 with the number of one or more respective memory blocks
5 having the one or more bad memory cells and the
6 corresponding size of addressable space of the memory block.

1 11. A reconfigurable memory comprising:
2 an array of memory cells; and
3 a reconfigurable memory controller to receive a logical
4 address and generate a physical address to address the array
5 of memory cells, the reconfigurable memory controller to map
6 out physical addresses of words having bad memory cells to
7 form a linear logical address space without addresses to
8 words of the bad memory cells.

1 12. The reconfigurable memory of claim 11, wherein,
2 the array of memory cells is organized into one or more
3 clusters, each of the one or more clusters having one or
4 more memory blocks.

1 13. The reconfigurable memory of claim 12, wherein,
2 the reconfigurable memory controller maps out the
3 physical addresses of memory blocks having bad memory cells.

1 14. The reconfigurable memory of claim 13, wherein,
2 the reconfigurable memory controller includes a
3 configuration register associated with each memory block,
4 each configuration register including an memory block enable
5 bit, the memory block enable bit to map out the respective
6 memory blocks having the bad memory cells.

1 15. The reconfigurable memory of claim 14, wherein,
2 each configuration register further includes a base
3 address associated with upper address bits of an address to
4 begin the physical addressing of a respective memory block
5 having all good memory cells.

1 16. The reconfigurable memory of claim 15, wherein,
2 the value of the base address is compared with the
3 value of the upper address bits of the address to determine
4 if each memory block having all good memory cells is
5 selected for access.

1 17. The reconfigurable memory of claim 16, wherein,
2 for a given memory block the comparison between the
3 value of the base address and the value of the upper address
4 bits of the address results in a match and the given memory
5 block is selected for access.

1 18. The reconfigurable memory of claim 11, wherein,
2 each memory block is a self contained memory unit
3 including an array of memory cells, an address decoder,
4 sense amplifier array, and tri-state data bus drivers.

1 19. An integrated circuit comprising:
2 a reconfigurable memory including
3 an array of memory cells,
4 and
5 a reconfigurable memory controller to receive
6 a logical address and generate a physical address
7 to address the array of memory cells, the
8 reconfigurable memory controller to map out
9 physical addresses of words having bad memory
10 cells to form a linear logical address space
11 without addresses to words of the bad memory
12 cells.

1 20. The integrated circuit of claim 19, wherein,

2 the array of memory cells is organized into one or more
3 clusters, each of the one or more clusters having one or
4 more memory blocks.

1 21. The integrated circuit of claim 19, wherein,
2 the reconfigurable memory controller of the
3 reconfigurable memory maps out the physical addresses of
4 memory blocks having bad memory cells.

1 22. The integrated circuit of claim 19, wherein,
2 the reconfigurable memory controller includes a
3 configuration register associated with each memory block,
4 each configuration register including a memory block enable
5 bit, the memory block enable bit to map out the respective
6 memory blocks having the bad memory cells.

1 23. The integrated circuit of claim 19, wherein,
2 the reconfigurable memory controller includes a memory
3 block base address.

1 24. The integrated circuit of claim 19, wherein
2 the integrated circuit is an application specific
3 integrated circuit.

1 25. The integrated circuit of claim 24 further
2 comprising:
3 a host port.

1 26. The integrated circuit of claim 24 further
2 comprising:
3 a memory test register; and
4 a built-in memory self-tester.

1 27. The integrated circuit of claim 24 further

2 comprising:

- 3 a memory test register;
- 4 a built-in memory self-tester; and
- 5 a test access port.

1 28. The integrated circuit of claim 24 further

2 comprising:

- 3 a host port;
- 4 a memory test register; and
- 5 a built-in memory self-tester.

1 29. A method of conserving power in an integrated
 2 circuit having parallel data buses, the method comprising:
 3 providing a bus keeper for each data bus in parallel
 4 together, the bus keeper to selectively keep the state of
 5 the bits of the respective data bus;
 6 addressing one of the bus keepers to select a new data
 7 input to change the state on a selected data bus; and
 8 maintaining the state on unselected data buses in
 9 parallel with the selected data bus to conserve power.

1 30. The method of claim 29, wherein,
 2 power is conserved by avoiding the discharging of bit
 3 lines having charged parasitic capacitance in each
 4 unselected data bus and by avoiding the charging of bit
 5 lines having discharged parasitic capacitance in each
 6 unselected data bus.

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